Patent ~~application S.N. 09/012,813 (TI-25311)~~ No. 6,182,203 and is incorporated herein by reference. A description of enhanced architectural features and an extended instruction set not described herein for CPU 10 is provided in co-assigned U.S. Provisional Patent application S.N. 60/183,527 ~~(TI-30302,~~ now U.S. Patent Application Serial No. 09/703,096 entitled *Microprocessor with Improved Instruction Set Architecture*~~)~~ and is incorporated herein by reference.--

a5

Rewrite the paragraph at page 10, lines 6 to 8 as follows:

--There are 32 valid register pairs for 40-bit and 64-bit data, as shown in Table ~~4~~ 1. In assembly language syntax, a colon between the register names denotes the register pairs and the odd numbered register is specified first.--

a6

Rewrite the paragraph at page 10, line 10 as follows:

a7 --Table ~~4~~ 1. 40-Bit/64-Bit Register Pairs--

MLC 11/19/2010

Rewrite the paragraph at page 10, lines ~~17 to 19~~ 13-16 as follows:

--Referring again to Figure 2, the eight functional units in processor 10's data paths can be divided into two groups of four; each functional unit in one data path is almost identical to the corresponding unit in the other data path. The functional units are described in Table ~~5.~~ 2.--

a8

Rewrite the paragraph at page 11, line 3 as follows:

a9 --Table ~~5.~~ 2. Functional Units and Operations Performed--

Rewrite the paragraph at page 12, lines 13 to 19 as follows:

--Table ~~6~~ 3 defines the mapping between instructions and functional units for a set of basic instructions included in the present embodiment. Table ~~7~~ 4 defines a mapping between

a10